

REMARKS

In response to an Advisory Action (Paper No. 18) mailed on February 28, 2003), Applicants have amended independent claims 1, 6 and 17, and respectfully believe that the claims are in condition for allowance. Upon entry of the amendments in this response, claims 1-2, 4-10, 17-18, 20 and 21 remain pending in the present application. These amendments and additions are specifically described hereinafter. It is believed that the foregoing amendments and additions add no new matter to the present application.

Claim 3 is canceled without prejudice, waiver, or disclaimer. Applicant takes this action merely to reduce the number of disputed issues and to facilitate early allowance and issuance of other claims in the present application. Applicant reserves the right to pursue the subject matter of these canceled claims in a continuing application, if applicant so chooses, and does not intend to dedicate any of the canceled subject matter to the public.

In the continuation sheet of the Advisory Action, the Examiner alleged that the Applicants' Admitted Prior Art hereinafter "AAPA" (Figs. 1-2) comprises an alignment link 30-33 for electrically connecting the first port with the second port; the alignment link comprises a signal buffer for buffering a signal traveling along the alignment link between the first port and the second port. In addition, the Examiner alleges that *Yoshitake* discloses an input driver 11 for outputting a signal; a buffer 12 for receiving an output of the driver 11 (Fig. 1, column 7, lines 10-20); wherein the driver 11 extends directly from the first area into the buffer 12 to provide a clock distribution circuit and can realize reduction in skew.

Applicants would like to point out that in the final Office Action mailed December 26, 2002 (Paper No. 16), the Office Action admitted that AAPA (Figs. 1 and 2) fails to disclose the first port extends directly into the common area from a first area. In this regard, the Office Action uses *Yoshitake* to allegedly disclose an input driver 11 for outputting a signal; a buffer 12 for receiving an output of the driver 11 (Fig. 1, column 7, lines 10-20), wherein the driver 11 extends directly from the first area into the buffer 12 to provide a clock distribution circuit and can realize reduction in skew. (Office Action at page 3, lines 5-13).

The present invention recognizes the difficulties and needs imposed by the prior art and puts forth a solution to overcome these previously unrecognized difficulties and needs. As part of integrated circuit design, various methodologies are utilized in laying out the signal wiring that forms the signal paths that transfer signals from one block of circuitry to another. Because of inherent differences in the methodologies that are used in laying out the signal wiring, it is common for there to be resulting mismatches in port alignments. As a result, the ports on the various blocks

of circuitry on an integrated circuit often do not precisely line up for easy and direct interconnection. Thus, efforts must be made to provide for an interface to link different blocks of circuitry. Further, in order to combat degradation in signal quality due to long signal paths, it is common to buffer the signals with buffering circuitry in order to retain proper signal timing and amplitude. Buffering of signals has typically been carried out separately from providing for linking of mis-aligned ports as is illustrated in Fig. 1 and Fig. 2 of the present application. This has resulted in integrated circuit real estate being utilized for aligning mis-aligned ports separately from integrated circuit real estate used for providing for appropriate signal buffering. This has meant greater usage of integrated circuit real estate.

Referring now to claim 1, Applicants respectfully submit that *Yoshitake* fails to teach, disclose, or suggest at least the element emphasized below.

Claim 1 recites:

1. An integrated circuit comprising:
 - a first port for outputting a signal;
 - a second port for receiving said signal;
 - a common area comprising an alignment link for electrically connecting said first port with said second port;
 - said first port is directly and electrically connected to said alignment link from a first area without the use of a first linking area that includes bridging traces for linking mis-aligned ports with said first port and said common area;
 - said second port is directly and electrically connected to said alignment link from a second area without the use of a second linking area that includes bridging traces for linking mis-aligned ports with said second port and said common area; and**
 - said alignment link comprises a signal buffer for buffering a signal traveling along said alignment link between said first port and said second port; said alignment link is arranged within said common area.

(Emphasis Added)

Applicants respectfully submit that *Yoshitake* fails to teach, disclose or suggest at least the above-emphasized element. In fact, the figures in *Yoshitake* appears to disclose a schematic view of a clock distribution circuitry for a semi-conductor integrated circuit. Applicants respectfully submit that *Yoshitake* fails to teach, disclose or suggest a physical layout and/or placement for aligning ports and providing for a signal buffering within a common area of integrated circuit real estate. In short, *Yoshitake* fails to teach, disclose or suggest “said second port is directly and electrically connected to said alignment link from a second area without the use of a second linking area that includes bridging traces for linking mis-aligned ports between said second port and said common

area,” as defined in claim 1. For this reason alone, Applicants respectfully submit that claim 1 is allowable.

Independent claim 6 includes “said second port is directly and electrically connected to said alignment link from a second area without the use of a second linking area that includes bridging traces for linking mis-aligned ports between said second port and said second port.” Applicants respectfully submit that the combination of AAPA and *Yoshitake* fails to teach, disclose or suggest at least the above-quoted element. In fact, as mentioned above with reference to claim 1, *Yoshitake* appears to disclose a schematic view of a clock distribution circuitry for a semi-conductor integrated circuit. Consequently, *Yoshitake* fails to disclose, teach or suggest a physical layout and/or placement of electrical components on a printed circuit board. Particularly, *Yoshitake* fails to teach, disclose or suggest “said second port is directly and electrically connected to said alignment link from a second area without the use of a second linking area that includes bridging traces for linking mis-aligned ports between said first port and said common area.” For this reason alone, Applicants respectfully submit that claim 6 is allowable.

Amended independent claim 17 includes “said second port is directly and electrically connected to said alignment means from a second area without the use of a second linking area that includes bridging traces for linking mis-aligned ports between said second port and said common area.” Applicants respectfully submit that the combination of AAPA and *Yoshitake*, fails to teach, disclose or suggest at least the above-quoted element. In fact, as mentioned above with reference to claim 1, *Yoshitake* appears to disclose a schematic view of a clock distribution circuitry for a semi-conductor integrated circuit. Consequently, *Yoshitake* fails to disclose, teach or suggest a physical layout and/or placement of electrical components on a printed circuit board. Particularly, *Yoshitake* fails to teach, disclose or suggest “said second port is directly and electrically connected to said alignment means from a second area without the use of a second linking area that includes bridging traces for linking mis-aligned ports between said second port and said common area.” For this reason alone, Applicants respectfully submit that claim 17 is allowable.

Newly added independent claim 21 includes “a second area arranged on said wiring level of said integrated circuit real estate, said second area includes a set of input ports that is electrically connected to said second set of wiring traces of said signal buffering blocks without the use of a second linking area that includes bridge traces for aligning mis-aligned ports between said second port and said common area.” Applicants respectfully submit that the combination of AAPA and *Yoshitake* fails to teach, disclose or suggest at least the above-quoted element. In fact, as mentioned above with reference to claim 1, *Yoshitake* appears to disclose a schematic view of a

clock distribution circuitry for a semi-conductor integrated circuit. Consequently, Yoshitake fails to disclose, teach or suggest a physical layout and/or placement of electrical components on a printed circuit board. Particularly, *Yoshitake* fails to teach, disclose or suggest "a second area arranged on said wiring level of said integrated circuit real estate, said second area includes a set of input ports that is electrically connected to said second set of wiring traces of said signal buffering blocks without the use of a second linking area that includes bridge traces for aligning mis-aligned ports between said second port and said common area." For this reason alone, Applicants respectfully submit that newly added claim 21 is allowable.

CONCLUSION

For at least the reasons set forth above, Applicants respectfully submit that pending claims i-2, 4-10, 17-18, 20 and 21 are in condition for allowance. Claim 3 has been cancelled. Favorable reconsideration and allowance of the present application and all pending claims is hereby respectfully requested. If, in the opinion of the Examiner, a telephonic conference would expedite the examination of this matter, the Examiner is invited to call the undersigned attorney at (770) 738-2378.

Respectfully submitted,

A handwritten signature in black ink, appearing to read "M. Paul Qualey, Jr.", is written over a horizontal line.

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**ANNOTATED VERSION OF MODIFIED CLAIMS TO
SHOW CHANGES MADE**

The following is a marked up version of the amended claims, wherein bracketing denotes deletions and underlining denotes additions.

1. (Twice Amended) An integrated circuit comprising:

a first port for outputting a signal;

a second port for receiving said signal;

a common area comprising an alignment link for electrically connecting said first port with said second port;

said first port [extends directly into said common area] is directly and electrically connected to said alignment link from a first area without the use of a first linking area that includes bridging traces for linking mis-aligned ports with said first port and said common area;

said second port [extends directly into said common area] is directly and electrically connected to said alignment link from a second area without the use of a second linking area that includes bridging traces for linking mis-aligned ports with said second port and said common area; and

said alignment link comprises a signal buffer for buffering a signal traveling along said alignment link between said first port and said second port; said alignment link is arranged within said common area.

6. (Twice Amended) An integrated circuit according to claim 1 wherein an integrated circuit comprising:

a first port located in a first area of integrated circuit real estate, for outputting a signal;

a second port located in a second area of integrated circuit real estate, for receiving said signal;

a common area comprising an alignment link for electrically connecting said first port with said second port;

said first port [extends directly into said common area] is directly and electrically connected to said alignment link from a first area without the use of a first linking area that

includes bridging traces for linking mis-aligned ports with said first port and said common area;

said second port [extends directly into said common area] is directly and electrically connected to said alignment link from a second area without the use of a second linking area that includes bridging traces for linking mis-aligned ports with said second port and said common area;

said alignment link comprises a signal buffer for buffering a signal traveling along said alignment link between said first port and said second port; and
said integrated circuit real estate comprises multi-levels.

17. (Twice Amended) An integrated circuit comprising:

a first port for outputting a signal;

a second port for receiving said signal;

a common area comprising an alignment means for electrically connecting said first port with said second port;

said first port[extends directly into said common area] is directly and electrically connected to said alignment means from a first area without the use of a first linking area that includes bridging traces for linking mis-aligned ports with said first port and said common area; and

said second port[extends directly into said common area] is directly and electrically connected to said alignment means from a second area without the use of a second linking area that includes bridging traces for linking mis-aligned ports with said second port and said common area.